REMARKS

Claims 1 through 22 are pending in this application. Claims 3-6, 15 and 16 are amended in several particulars for purposes of clarity in accordance with current Office policy, to assist the examiner and to expedite compact prosecution of this application. Claims 21 and 22 have been newly added.

I. Claim Rejections - 35 USC § 112

The Examiner states that Claims 3-6,15, and 16 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

The Examiner states that in line 3 of each of claims 3-6, 15, and 16, "polysilicon" has no antecedent basis. The Examiner states that it is clear from the claims that each of these "polysilicons" has a thickness and is formed by SPC or ELA methods, as the case may be and what is indefinite is where the antecedent basis of "polysilicon" resides. The Examiner states that the specification states that the "activation layer" of claims 1 and 13 is activated by either the ELA or SPC methods, so it seems likely that the antecedent of "polysilicon" is "an activation layer." In the examiner's opinion there is nothing wrong with describing the ELA and SPC methods using their acronyms. The Examiner states that there are literally tens of thousands of documents available in the prior art to teach one having skill in the art what these acronyms mean, and how to practice the methods so referred to.

Therefore, the claims have been amended according to the Examiner's suggestion. Paragraphs 37-38 for example supports such an amendment for clarification purposes only.

Concerning the acronyms, to avoid any confusion with other similar terms in the art, the Applicant believes it would be more definite to define the acronym in the claim.

II. Claim Rejections - 35 USC § 102

No claim is anticipated under 35 U.S.C. §102 (b) unless all of the elements are found in exactly the same situation and united in the same way in a single prior art reference. As mentioned in the **MPEP §2131**, "a claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference." Verdegaal Bros. v. Union Oil Co. of California, 814 F.2d 628, 631, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Every element must be literally present, arranged as in the claim. *Richardson v. Suzuki Motor Co.,* 868 F.2d 1226, 9 USPQ2d 1913, 1920 (CAFC 1989). The identical invention must be shown in as complete detail as is contained in the patent claim. *Id.*, "All words in a claim must be considered in judging the patentability of that claim against the prior art." *In re Wilson,* 424 F.2d 1382, 165 USPQ 494, 496 (CCPA 1970), and MPEP 2143.03.

A. Claims 1, 2, 4, 6, 13, 14, and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Busta (4,949,141). The Applicant respectfully traverses.

1. With regard to claims 1, 2, 4, and 6 the Examiner states that Busta discloses a thin film transistor comprising a buffer layer 12-32 formed on a substrate 10; an 8000 angstrom thick (Note column 5 line 9. The thickness of the activation layer 34 must be known to know whether the reference meets the claims) activation layer 34 formed on said buffer layer 12-32; and a gate insulation layer 40 having a thickness of at least 1,000 angstroms (1200-2000 angstroms, see column 5 line 20) formed on said substrate 10 including said activation layer 34, with said buffer layer 12-32 having a 750 angstrom (column 5 line 9 discloses a 500-1500 angstrom range) step 32 (the size of the step 32 is defined by projecting buffer layer part 32. The Examiner further states that the projecting part and the step 32 it creates will be interchangeably referred to as part "32") formed between a lower part of said activation layer 34 and a part except said lower part of said activation layer 34, said 750 angstrom step 32 being a half or less of the thickness sum (the sum of 8000, activation layer 34, and 1000, gate insulation layer 40, being 9000) of said activation layer 34 and gate insulation layer 40, and further comprising a 500 (500-1500 angstroms, note column 5 line 9) angstrom polysilicon layer 36. The Examiner notes (figure 2B) that the thickness of the gate insulation layer 40 is not changed on said sidewall of said buffer layer 12-32 (the side wall of the buffer layer 12-32 is the sidewall of the step 32 portion of the buffer layer 12-32). Therefore, the Examiner states that the buffer layer 12-32 must have a step 32 to such a degree as to accomplish this visible result. The Examiner further notes figure 2B, column 4 lines 50-51, and column 5 lines 9, 10, and 20 of Busta.

a. However, concerning claims 1 and 13, reference 32 is clearly not the buffer layer as

claimed in the present invention. Claim 1 states that the buffer layer is formed on a substrate with a separate activation layer formed on the buffer layer.

In the Examiner's response to the arguments, the Examiner argues the semantics of the Applicant remarks of "can" and makes the point that therefore for examination purposes it will be assumed reference 32 may be included in either the buffer layer or the activation layer.

However, this point is not relevant to the rejection itself. It is the reference that must be looked at and in the reference Busta, reference 32 is not a buffer layer or activation layer. Instead, Busta shows that references 12-32 are clearly NOT the buffer layer and therefore, the rejection is flawed.

Reference 12 is stated clearly in Busta as being a pixel element and reference 32 is clearly the drain layer. Therefore, neither reference 12 or 32 is the buffer layer.

It is the buffer layer in the present invention that has the step formed between a lower part of the activation layer and a part except the lower part of the activation layer. Paragraph 31 of the present invention states that a buffer layer 210 (diffusion barrier) is formed on a glass substrate 200 to prevent impurities such as metal ions diffused from the glass substrate 200 from infiltrating into the activation layer of polycrystalline silicon. However, in Busta, pixel element 12 is stated as being a tin oxide layer and drain 32 is of a-n+Si:H. Clearly, neither pixel element 12 and drain 32 are not the buffer layers.

b. Concerning claims 1 and 13, further, it is improper for the Examiner to say that

buffer layer 12-32 has step 32 since pixel element 12 is separate from the drain 32. The present invention claims the buffer layer having a step formed, and not a pixel layer having a drain 32 which is being construed as a buffer layer.

c. Concerning claims 1 and 13, Busta fails to disclose the step of the buffer layer being a half or less of the thickness sum of said activation layer and gate insulation layer because drain 32 is not a buffer layer. Moreover, drain 32 is different than pixel element 12 and the two different layers should not be combined together as a single buffer layer.

d. Concerning claims 2 and 14, Busta fails to disclose the buffer layer having a step to such a degree that the thickness of the gate insulation layer in not changed or even on the side wall of the buffer layer. There must be an actual disclosure in Busta concerning the unchanged thickness of the gate insulation as related to the step in the buffer layer. However, Busta only states that gate insulator layer 40 1200-2000 Angstroms thick. Therefore, not only does Busta not disclose an unchanged thickness, but in fact it states it can vary from 1200 to 2000 Angstroms, thereby indicating that the thickness does change. Furthermore, there is no specific disclosure concerning the sidewall of the buffer layer.

Further, the Examiner cannot rely on the drawings to show the unchanged thickness as there is no related disclosure in the specification indicating as such. Specifically in the **MPEP §2125** under the heading "DRAWINGS AS PRIOR ART" and under the subheading "PROPORTIONS OF FEATURES IN A DRAWING ARE NOT EVIDENCE OF ACTUAL PROPORTIONS WHEN

DRAWINGS ARE NOT TO SCALE", the MPEP states "When the reference does not disclose that the drawings are to scale and is silent as to dimensions, **arguments based on measurement of the drawing features are of little value**. However, the description of the article pictured can be relied on, in combination with the drawings, for what they would reasonably teach one of ordinary skill in the art. *In re Wright*, 569 F.2d 1124, 193 USPQ 332 (CCPA 1977).

Here, Busta never states that the gate insulator layer has the thickness unchanged, especially on the sidewall of the buffer layer in the specification and therefore, there is no description to be relied on in combination with the drawings.

e. Concerning claims 4, 6, 16, the thickness of the activation layer being 500 Angstroms and the step being 750 Angstroms and the gate insulation layer being at least 1000 Angstroms is not disclosed since layer 34, which the Examiner states is the activation layer is disclosed to be 8000-15000 Angstroms. 500 Angstroms is not within the range of 8000-15000.

The statement by the Examiner concerning product by process claims and the relevant weight of the method claims or intermediate products is not germane to the ELA polysilicon and SPC polysilicon because it is the polysilicon that is used as the activation layer as mentioned in the claim and in paragraphs 37 and 38 and therefore, the thickness of the activation layer is important.

f. Concerning claims 4, 6 and 16, there is no disclosure in Busta that there is a step of 350 Angstroms in the activation layer. There is no disclosure as to the size of the step, but rather only a disclosure of 8000-15000 Angstroms of the thickness only.

B. Claims 1, 2, 13, and 14 are rejected under 35 U.S.C. 102(b) as being anticipated by Adachi et al. (5,985,704). The Applicant respectfully traverses.

1. With regard to claims 1, 2, 13 and 14, the Examiner states that Adachi et al. discloses a thin film transistor with a buffer layer 22 (12 in figure 1) formed on a substrate 21 (11); a 1000-1500 angstrom activation layer 13 (23 in figure 2) formed on said buffer layer 22 (12 in figure 1); and a 300 angstrom gate insulation layer 29 formed on said substrate 21 (11) including said activation layer 13 (23 in figure 2), with said buffer layer 22 (12 in figure 1) having a step "y" formed between a lower part of said activation layer 13 (23 in figure 2) and a part except said lower part of said activation layer 13 (23 in figure 2), the step "y" in the buffer layer 22 (12 in figure 1) having such a degree that thickness of the gate insulation layer 29 is not changed on said side wall of said buffer layer 22 (12 in figure 1) and being 80-500 angstroms thick and thus a half or less of the thickness sum (1000-1500 plus 300 angstroms) of said activation layer 23 (1000-1500 angstroms thick) and gate insulation layer 29 (300 angstroms thick). The Examiner notes figures 1A-1E, 2A-E, column 4 lines 1-5 and 20-24, and column 8 lines 1-5,18-24, and 41-55 of Adachi et al.

a. Concerning claims 1 and 13, the Examiner has stated that it is only the final product that is important in the claim and yet, the Examiner refers to layers in the interim process. For example references 13 and 23 are the amorphous silicon film during the process and not the activation layer as claimed in the present invention.

Further, it is not clear that 13, 23, the amorphous silicon film is the activation layer in a final product.

b. The measurement and comparison of the thickness are not proper disclosures given by the Examiner for the comparsion as they relate to the interim process and not the final product or are not properly given. Therefore, Adachi fails to disclose the step being up to half of the thickness sum of the activation layer and gate insulation layer.

For example, the Examiner states that the activation layer 13, 23 is between 1000-1500 Angstroms, but Adachi states that "an amorphous silicon film 13 is deposited on the silicon oxide film 12 by a plasma CVD to a thickness of 500.ANG. to 1500.ANG., for example, 1000.ANG." The measurements are of the interim material used and not in the final product.

The Examiner states that gate insulation layer is 300 Angstroms. However, no such disclosure is ever given in Adachi. Adachi only refers to a gate insulation layer 29 and that is all.

c. Concerning claims 2 and 14, the Examiner improperly relied on the drawing of figure 1 to state that the side wall of the gate insulation layer is not changed. The Specification of Adachi never states that the drawings are to scale and it never states an actual disclosure that the side walls are even. Therefore, as shown above, therere is no disclosure the even thickness of the side wall of the gate insulation layer.

III. Claim Rejections - 35 USC § 103

According to MPEP 706.02(j), the following establishes a *prima facie* case of obviousness under 35 U.S.C. §103:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art and not based on applicant's disclosure. In re Vaeck, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

A. Claims 3, 5, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adachi et al. (5,985,704) in view of Yamazaki et al. (2004/0211356). The Applicant respectfully traverses.

The Examiner states that Adachi et al. discloses a thin film transistor with all the limitations of claims 3, 5, and 15, including that the step be 350 angstroms (Adachi et al. disclose 80-500 angstroms) in the activation layer, except that the thickness of the gate insulation layer be at least 400 (400 angstroms or more) angstroms and that the activation layer comprise polysilicon having a thickness of 300 angstroms. The Examiner notes that figures 1A-1E, 2A-E, column 4 lines 1-5 and 20-24, and column 8 lines 1-5, 18-24, and 41-55 of Adachi et al.

However, Yamazaki et al. discloses a thin film transistor with that a thickness of a gate insulation layer 405 that is 400 angstroms or more (1000-1500 angstroms) and an activation layer 403 comprising KrF excimer laser activated polysilicon having a thickness of 300 angstroms. Note figures 7A-D, 10A-C, and paragraphs 0088-0098 of Yamazaki et al. Therefore, it would have been obvious to a person having skill in the art to modify the dimensions of the of Adachi et al.'s thin film transistor to the dimensions taught by Yamazaki et al. in order to increase gate-channel breakdown voltage by thickening the gate insulating film, while at the same time making it easier to fully deplete the channel, by making the channel shallower, to thus provide a TFT able to perform over a wider range of voltages.

1. However, the Examiner is using measurements from interim products as paragraph 8 of Yamazaki states that "For example, after an active layer (in which a channel formation layer is formed) for an insulated-gate field-effect transistor is formed, a silicon oxide film becoming a gate-insulating film is formed." Further, Yamazaki states that reference 405 is only the silicon oxide film. Therefore, the measurement is not of the final product and therefore, the disclosure is not made.

2. Further, the Examiner states that the polysilicon of the activation layer is 300 Angstroms is taught in Adachi. However, a search of Adachi shows no such disclosure relating to 300 Angstroms of the polysilicon of the activation layer.

3. The references fail to disclose a step 350 Angstroms in the activation layer as reference 23 is not even shown to have a step, but rather is a flat surface. A thickness of 8--500 angstroms of the surface does not mean the step is of such measurement. Only the thickness is actually taught or suggested and no step within the activation layer is taught or suggested.

4. The Examiner states the following that it should be noted that Busta discloses a TFT designed for vertical current flow, as opposed to lateral flow. The Examiner states that Adachi and Yamazaki TFTs are lateral TFTs. However, the Examiner states that as Adachi points out, a 500-angstrom step is an extremely tall step for a lateral TFT. Without extreme care laying down the gate insulating layer (for example, laying down two or more separate insulating layers) a short may be generated at the side surface of the activation layer when the buffer layer is etched so deeply as to make a 500-angstrom step. The Examiner further states that yet applicant's claims 4, 6, and 16 require a 750-angstrom step. The Examiner states that to accomplish such a very extreme step, it is safer to build a vertical TFT, such as taught by Busta, where the gate, and the gate insulator, is essentially laid down on the side of the step.

However, the Examiner's argument above is showing that the references are teaching away from the present invention and therefore, should not be combined. According to MPEP §2145, "It

is improper to combine references where the references teach away from their combination. *In re Grasselli*, 713 F.2d 731, 743, 218 USPQ 769, 779 (Fed. Cir. 1983). This portion of the references cannot be just ignored because according to MPEP §2141.02, "A prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984)."

5. The Examiner states that the motivation to combine the references is to increase gate-channel breakdown voltage by thickening the gate insulating film, while at the same time making it easier to fully deplete the channel, by making the channel shallower, to thus provide a TFT able to perform over a wider range of voltages. However, this does not relate to the inclusion of the thickness of the gate insulation layer specifically. "Combining prior art references without evidence of such a suggestion, teaching, or motivation simply takes the inventor's disclosure as a blueprint for piecing together the prior art to defeat patentability. *In re Dembiczak*, 175 F.3d 994, 50 USPQ.2d 1614 (Fed. Cir. 1999). The showing must be "clear and particular" without broad generalized conclusory statements. *Id.* There must be specific statements showing the scope of the suggestion, teaching, or motivation to combine the prior art references. *Id.* at 1000. There must be an explanation to what specific understanding or technical principle would have suggested the combination of references. *Id.* Here, the motivation to combine is not clear and particular as related to the present invention as the reasoning is not clear and particular.

The Federal Circuit has mentioned that "[t]he test for obviousness is not whether the features

of one reference may be bodily incorporated into another reference...Rather, we look to see whether combined teachings render the claimed subject matter obvious." *In re Wood*, 599 F.2d 1032, 202 USPQ 171, 174 (CCPA 1979) (citing *In re Bozek*, 416 F.2d 1385, 1390, 163 USPQ 545, 549-50 (CCPA 1969); *In re Mapelsden*, 329 F.2d 321, 322, 141 USPQ 30, 32 (CCPA 1964). Here, respectfully, the Examiner is using the present invention as a blue print to piece together a rejection.

IV. Newly Added claims

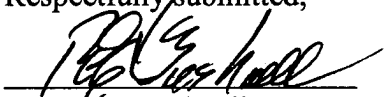
Claims 21 and 22 are not anticipated or obvious with regard to the applied art. The art fails to teach or suggests wherein a thickness of the gate insulation layer is at least 400 Å when a thickness of said activation layer is 300 Å and step is 350 Å in said activation layer and the step of said buffer layer being formed on a single body of said buffer layer with the step protruding from a flat portion of said buffer layer and the step of said activation layer being formed on a single body of said activation layer with the step of said activation layer protruding from a flat portion of said activation layer.

Claims 21 and 22 are supported by the entirety of the drawings and the related disclosure including for example figure 3.

In view of the foregoing amendments and remarks, all claims are deemed to be allowable and this application is believed to be in condition to be passed to issue. If there are any questions, the examiner is asked to contact the applicant's attorney.

A fee of $100.00 is incurred by this Amendment for the addition of two (2) claims above twenty (20). Applicant's check drawn to the order of the Commissioner accompanies this Amendment. Should there be a deficiency in payment, or should other fees be incurred, the Commissioner is authorized to charge Deposit Account No. 02-4943 of Applicant's undersigned attorney in the amount of such fees.

Respectfully submitted,



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